Claims

I claim:

1. A semiconductor device comprising:

a semiconductor substrate comprising a region of a first conductivity type, a top electrode being in electric contact with a top surface of said substrate, a bottom electrode being in electrical contact with a bottom surface of said substrate;

a field shield region of a second conductivity type, said field shield region being laterally bounded by dielectric sidewalls, said dielectric sidewalls separating said field shield region from said region of the first conductivity type, said field shield region being bounded from below by a PN junction with said region of the first conductivity type; and

a shield electrode in electrical contact with the field shield region and with the top electrode.

2. The device of Claim 1 wherein the electrical contact between the control electrode and the field shield region is ohmic.

3. The device of Claim 1 wherein the electrical contact between the top electrode and the top surface is ohmic.

4. The device of Claim 1 wherein the electrical contact between the top electrode and the top surface comprises a Schottky barrier.

5. The device of Claim 1 wherein the electrical contact between the bottom electrode and the bottom surface is ohmic.

6. The device of Claim 1 wherein the electrical contact between the bottom electrode and the bottom surface comprises a Schottky barrier.

7. The device of Claim 1 comprising a vertical JFET with ohmic bottom and top electrodes.

8. The device of Claim 1 wherein the contact between the top electrode and the top surface of said substrate is a Schottky barrier contact and the contact between the bottom electrode and the bottom surface of said substrate is ohmic.

9. A device comprising:

a semiconductor body comprising a region of a first conductivity type;

a groove formed in the region of first conductivity type;

a dielectric layer lining the surfaces of the groove;

a conductive material in the groove, the conductive material being bounded by the gate dielectric layer; and

a field shield region of a second conductivity type located below the groove, the lateral sides of the field shield region being bounded by dielectric sidewalls, the dielectric sidewalls being interposed between the field shield region and the region of first conductivity type; the bottom of said field shield region being bounded by PN junction between said field shield region and said region of first conductivity type.

10. The device of Claim 9 wherein the groove is "V" shaped.

11. The device of Claim 9 wherein the groove is "U" shaped.

12. The device of Claim 9 wherein the dielectric layer is formed of SiO_2.

13. The device of Claim 9 wherein the dielectric layer is formed of Si_3N_4.

14. The device of Claim 9 wherein the conductive material comprises heavily-doped polysilicon.

15. The device of Claim 14 wherein the conductive material comprises silicide.

16. A trench-gated semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer formed on the substrate;

first and second trenches formed in the epitaxial layer, said first and second trenches being separated by a mesa;

a gate dielectric layer lining the walls and floor of each of the trenches;

a gate electrode in each of the trenches, the gate electrode being bounded by the gate dielectric layer;

a body region of a second conductivity type in the mesa;

a source region of the first conductivity type adjacent a wall of the trench and the top surface of the epitaxial layer;

a drift region of the epitaxial layer located below the body region and being doped with material of the first conductivity type;

a field shield region of a second conductivity type located below each of the trenches, the lateral sides of the field shield region being bounded by dielectric sidewall spacers, the dielectric sidewall spacers being interposed between the field shield region

and the drift region of the epitaxial layer, the field shield region being bounded from below by a PN junction; and

a metal layer on top of the epitaxial layer and in electrical contact with the source region and the body region;

wherein the field shield region is electrically connected to the source region and the body region.

17. The device of Claim 16 wherein the dielectric sidewall spacers comprise silicon dioxide.

18. The device of Claim 16 wherein the gate dielectric layer comprises silicon nitride

19. The device of Claim 16 further comprising a body contact region of the second conductivity type adjacent a top surface of the mesa.

20. The device of Claim 16 wherein the field shield region is electrically connected to the source and body regions by means of the metal layer and a well of the second conductivity type.

21. The device of Claim 16 wherein said mesa is hexagonal when viewed from above, the device comprising a plurality of said hexagonal mesas.

22. The device of Claim 16 wherein said mesa is square when viewed from above, the device comprising a plurality of said square mesas.

23. The device of Claim 16 wherein said mesa is circular when viewed from above, the device comprising a plurality of said circular mesas.

24. The device of Claim 16 wherein said mesa is in the form of a longitudinal stripe, the device comprising a plurality of said mesas arranged parallel to each other.

25. The device of Claim 16 wherein said device is a MOSFET.

26. The device of Claim 16 wherein said device is an insulated gate bipolar transistor

27. A trench-gated semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer formed on the substrate;

first and second trenches formed in the epitaxial layer, said first and second trenches being separated by a mesa;

a gate dielectric layer lining the walls and floor of each of the trenches;

a gate electrode in each of the trenches, the gate electrode being bounded by the gate dielectric layer;

said mesa comprising:

a body region of the second conductivity type;

a source region of the first conductivity type adjacent a wall of the trench and the top surface of the epitaxial layer; and

a field shield region of a second conductivity type extending downward from the top surface of the epitaxial layer, the lateral sides of the field shield region being bounded by dielectric sidewall spacers, the field shield region being bounded from below by a PN junction;

a drift region of the epitaxial layer located below the body region and being doped with material of the first conductivity type; and

a metal layer on top of the epitaxial layer and in electrical contact with the source region, the body region and the field shield region.

28. A termination region in a power semiconductor device die, said termination region being formed in region of the first conductivity type and comprising:

a plurality of trenches, said trenches being parallel to each other and being parallel and adjacent to an edge of the die, each of said trenches having a sidewall and a floor lined with a dielectric layer, each of said trenches comprising a layer of a conductive material, said conductive material being insulated from the region of first conductivity type by said dielectric layer; and

a field shield region directly below each of said trenches, said field shield region being doping with material of a second conductivity type, said field shield region being bounded laterally by a dielectric spacer and being insulated from said conductive material by said dielectric layer, the field shield region being bounded from below by a PN junction;

wherein said conductive material in each of said trenches is electrically insulated from said conductive material in the other ones of said trenches.

29. A method of fabricating a trench-gate semiconductor device comprising:

providing a semiconductor substrate of a first conductivity type;

forming an epitaxial layer of the first conductivity type on the substrate;

forming first and second trenches in the epitaxial layer, the first and second trenches being separated by a mesa;

forming dielectric spacers on the sidewalls of the trenches;

filling a bottom portion of the trenches with a semiconductor material of a second conductivity type;

removing portions of the dielectric spacers above the semiconductor material of the second conductivity type;

forming a dielectric layer on the walls of the trenches above the semiconductor material of the second conductivity type and on the top surface of the semiconductor material of the second conductivity type; and

filling an upper portion of the trenches with a conductive gate material.

30. The method of Claim 29 comprising forming a body region of the second conductivity type in the mesa and forming a source region of the first conductivity type in the mesa, both the body region and the source region abutting a wall of the first trench.

31. The method of Claim 29 wherein forming the source region comprises implanting a dopant of the first conductivity type through an opening in a first mask layer formed above a surface of the epitaxial layer.

32. The method of Claim 29 comprising:

depositing a second dielectric layer over the surface of the epitaxial layer and the conductive gate material; and

removing a first portion of the second dielectric layer, leaving a second portion of the dielectric layer above the conductive gate material and a portion of the source region and forming an opening in said second dielectric layer above a portion of the mesa.

33. The method of Claim 32 comprising implanting a dopant of the second conductivity type through the opening in the second dielectric layer to form a body contact region in the mesa.

34. The method of Claim 32 wherein forming the source region comprises:

forming a second dielectric layer above the conductive gate material;

depositing a polysilicon layer doped with a dopant of the first conductivity type over the second dielectric layer and over the mesa;

etching the polysilicon layer directionally so as to leave a polysilicon spacer on a sidewall of the second dielectric layer; and

heating the polysilicon spacer to cause the dopant of the first conductivity type in the polysilicon spacer to diffuse into the epitaxial layer.

35. The method of Claim 34 wherein forming the source region comprises:

forming a second dielectric layer above the conductive gate material;

introducing a dopant of the first conductivity type through the top surface of the mesa to form a source layer;

depositing a polysilicon layer doped with a dopant of the first conductivity type over the second dielectric layer and over the mesa;

etching the polysilicon layer directionally so as to leave a polysilicon spacer on a vertical surface of the second dielectric layer; and

removing a portion of the source layer while leaving in place a remaining portion of the source layer, at least part of the remaining portion of the source layer being located under the polysilicon spacer.

36. The method of Claim 29 comprising depositing a third dielectric layer over the second dielectric layer and the polysilicon spacer and directionally etching the third dielectric layer on a vertical surface of the polysilicon spacer.

37. A method of fabricating a power MOSFET comprising:

growing an epitaxial layer on a semiconductor substrate, both said epitaxial layer and said substrate being doped with material of a first conductivity type;

forming a first mask on a surface of said epitaxial layer, said first mask having an opening where a trench is to be formed;

etching said epitaxial layer through said opening in said first mask to form a trench in said epitaxial layer;

forming a first dielectric layer on the sidewalls and a bottom of said trench;

removing a portion of said first dielectric layer on the bottom of said trench;

depositing a second epitaxial layer doped with material of a second conductivity type in a lower portion of said trench so as to form a field shield region;

removing a second portion of said first dielectric layer on the sidewalls of said trench above said second epitaxial layer, thereby forming a dielectric spacers on the sides of said field shield region;

forming a second dielectric layer on the exposed portions of the sidewalls of the trench and on a top surface of said field shield region;

filling said trench with a first polysilicon layer;

removing a portion of said first polysilicon layer such that a surface of said first polysilicon layer is located at a level below a top surface of said first mask, thereby forming a polysilicon gate;

depositing a glass layer on said first mask and said polysilicon gate;

planarizing said glass layer such that a surface of said glass layer is coplanar with the top surface of the first mask, thereby forming a glass plug directly above said polysilicon gate;

removing at least a portion of the first mask;

implanting dopant of the second conductivity type to form a body region in said epitaxial layer;

depositing a second polysilicon layer over a top surface of said glass plug and said epitaxial layer, said second polysilicon layer being doped with material of said first conductivity type;

etching said second polysilicon layer directionally so as to form a polysilicon spacer on a sidewall of said glass plug;

heating said polysilicon spacer so as to cause dopant of said first conductivity type to diffuse from said polysilicon spacer into said epitaxial layer, thereby creating a source region;

depositing a metal layer over said glass plug and said first epitaxial layer;

forming a second mask over said metal layer; and

etching said metal layer through an opening in said second mask to form a source metal section of said metal layer.